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Integrated Circuit Signal Measurements Using an Undersampling Approach

R. Mason, B. Simon, and K. Runtz

***Abstract*—Integrated circuit (IC) manufacturing processes have been successful in introducing complex high-speed analog and mixed-signal devices. Testing these devices is becoming increasingly difficult. The paper presents a novel method of analyzing analog IC’s using periodic input stimuli and wide-band undersampling. In its simplest form, the testing procedure can be implemented in a design by adding an analog switch to sample the response signal at a particular node under test and a buffer to bring the sampled values off-chip. Using a sequential undersampling algorithm to control the switch allows high-frequency signals to be mixed down in frequency and driven off-chip using a low bandwidth buffer. By placing the sampling circuit on-chip, the high-frequency buffering problems associated with a similar system using digital sampling scopes or mixed-signal IC testers can be avoided. The utility of the procedure has been illustrated by measuring the frequency response, slew rate, and transient response characteristics for a unity gain 1.2-μm CMOS opamp.**

***Index Terms*—High speed, IC measurements, mixed signal, undersampling.**

I. INTRODUCTION

Advances in integrated circuit (IC) processing technologies have enabled the development of complex high-speed analog and mixed-signal devices [1]–[3]. Process advances have resulted in a steady increase in circuit density and speed. Although mixed-signal technologies have become a popular solution to many design problems, current testing technologies are inadequate for accessing high-frequency analog signals on-chip [2], [3].

A common testing procedure used to determine the signal level at a particular node is to buffer the signal off-chip [4]. Some of the problems with this approach include: 1) intrinsic parasitic capacitance of the buffer input stage and metal interconnect will load the node under test; 2) one output pin is required for each test node unless some form of multiplexing is used (multiplexing introduces additional parasitics and limits the frequency response); and 3) the large load on the output pin can severely limit the high-frequency response.

Another common approach used to test analog IC’s is circuit probing [5]–[7]. Contact probing techniques have problems similar to those encountered with off-chip buffering. The node under test is loaded by the parasitic characteristics of the probe testing apparatus and the on-chip probe pad [5], [6]. Noncontact probing technologies can significantly reduce loading [7], however, they are generally not suitable for production tests where high pin counts and high throughput are required.

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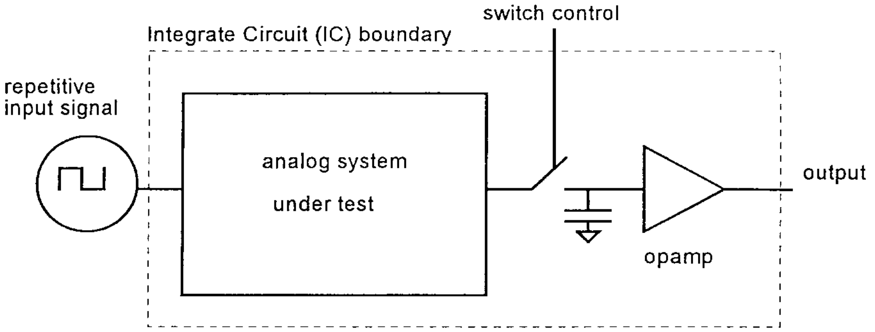


Fig. 1. Tester block diagram.

This paper presents a novel approach to high-frequency analog signal testing. The approach is based upon wide-band undersampling techniques similar to those used in sampling oscilloscopes and mixed-signal IC testers [8], [9]. What is unique is that the sampler is constructed on-chip where the signal being tested can be mixed down to a lower frequency before being brought off-chip. Using our approach we can avoid: 1) the high-frequency response limitations of the off-chip driver; 2) the large power, noise, and circuit area required for a high-speed buffer; and 3) the potentially larger test node loading associated with a high-speed buffer. We can also incorporate a number of undersamplers on-chip and time multiplex their signals to examine multiple internal nodes with minimum silicon overhead.

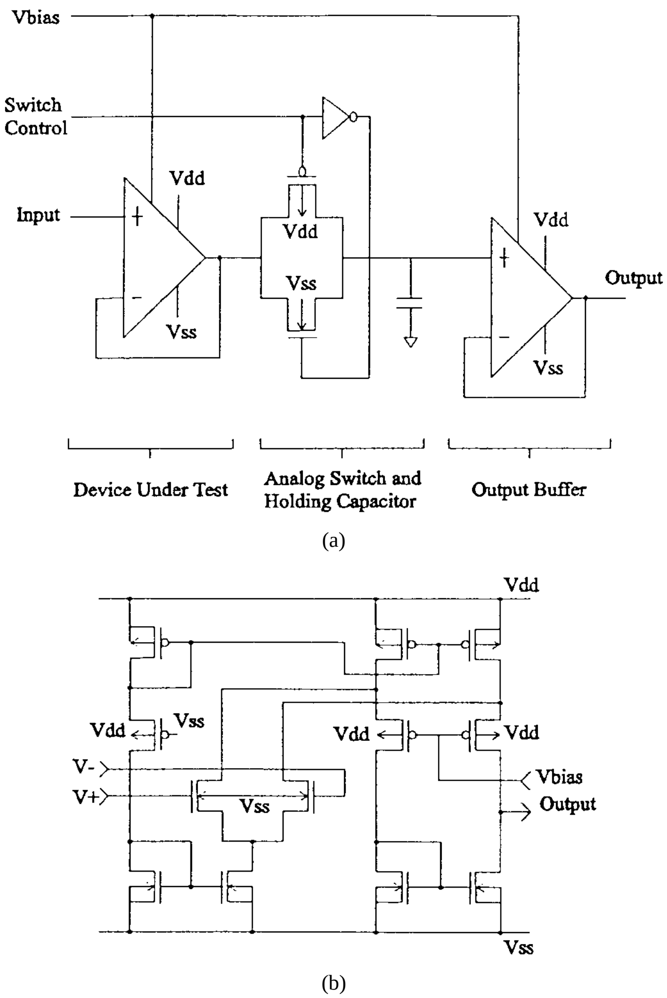
II. Analog Signal Tester Design

An IC testing procedure has been developed for high-frequency analog signals. In its simplest form, two components are required on-chip to carry out the test procedure (see Fig. 1). The first component is an analog switch which is used to sample an input signal. The switch also includes a storage capacitor to hold the sampled values. The second component is an opamp buffer which brings the sampled values off-chip where they can be stored and/or displayed.

There are four key elements to the procedure: 1) repetitive input signals; 2) narrow pulse on switch control to provide trickle charge; 3) small frequency shift between the input signal and the switch control, and 4) on-chip holding capacitor to integrate trickle and minimize charge coupling from the switch control signal.

By applying a repetitive input signal of known frequency, the response of the analog system will also be repetitive. If the sample frequency is close to the input frequency, the input signal will be undersampled and the frequency response of the off-chip buffer can be greatly reduced. Narrow pulses (typically 2 ns) are applied to the switch control signal which allows a small amount of charge to pass through the switch on each pulse. By using minimum geometry transistors and a small trickle charge, loading on the internal node can be minimized (~10 fF).

The on-chip holding capacitor is used to integrate the trickle charge through the analog switch. The capacitor is also used to reduce charge injection error due to capacitive coupling between the switch control signal and the output of the analog switch. The use of smaller sampling switches would further reduce the capacitive coupling and charge injection error.



(a)

(b)

Fig. 2. Schematics for (a) IC and (b) two-stage opamp.

An IC was designed to test the undersampling approach. The chip was designed using Cadence design tools and fabricated using NORTEL's 1.2-μm CMOS process which was provided through the Canadian Microelectronics Corporation (CMC). The IC contained two externally compensated two-stage opamps which were used as the output buffer and as the device under test (DUT). A CMOS transmission gate and inverter were used as the analog switch. Schematics for the IC and the individual opamps can be seen in Fig. 2(a) and (b). The total silicon area occupied by the test circuitry (output buffer, holding capacitor, and sampling switch) is 224 μm × 78 μm.

III. Simulation and Experimental Results

The IC was simulated using HSPICE and level 2 models provided by the CMC. A high-speed data generator (HP E2900) was used to

TABLE I
RISING EDGE SQUARE WAVE RESPONSE

Parameter	Simulated	Measured
Slew Rate (rising edge)	160 V/μs	148 V/μs
Overshoot (% of input voltage)	9.8%	6.8%
Settling Time (to within 1% of final value)	19 ns	38ns

TABLE II
TEST RESULTS FOR FIRST PROTOTYPE IC

Parameter	Measured Value
Opamp 3dB Bandwidth (100 mVpp sinusoid)	200 MHz
Opamp Slewrate (1.2Vpp square wave input signal)	+148 V/μs, -108 V/μs
Total Harmonic Distortion (10 MHz input sinusoid)	-68 dB
Noise Voltage	86 nV/Hz$^{1/2}$
Input - Output Isolation (10 MHz input sinusoid)	-51 dB
Switch Control - Output Isolation (10 MHz input sinusoid)	-53 dB

generate sampling pulses on the switch control input. Sinusoidal input signals were generated by an RF signal generator (HP8648). Square wave input signals were generated by a high-speed GaAs switch (Mini-Circuits ZYSW-2-50DR) which was driven by a low-frequency function generator (HP33120A). Output signals were measured using a digital scope (TDS684) or network/spectrum analyzer (HP4195A).

A sinusoidal frequency sweep was conducted on the IC to provide the frequency response characteristic of the on-chip opamp. In the first test, the sampling switch was closed continuously. The simulation and experimental results showed a 3-dB bandwidth of approximately 1.6 MHz. The limited frequency response is due to the off-chip loading of the output buffer.

The sampling switch is driven by a 2-ns pulse waveform with a repetition rate which is slightly offset from the sinusoidal input signal (i.e., the input signal is undersampled using a trickle charge technique). The 3-dB bandwidth is increased to 200 MHz for the sampled signal which is no longer limited by the off-chip loading and is, in fact, a measure of the frequency response of the DUT with a small amount of internal loading. With the sampling switch being closed only momentarily, the loading on the DUT is primarily due to routing parasitics and the parasitic capacitance of the sampling switch input. By placing the sampling switch close to the DUT and using minimum geometry transistors in the sampling switch, the test circuitry loading can generally be kept small compared to the normal loading of the on-chip node. The measured 3-dB bandwidth was 12% lower than the simulated results. This is believed to be primarily due to the accuracy of HSPICE transistor models.

Transient response characteristics for the DUT were measured using a square wave input. The rising edge square wave response was compared to the simulated response using a 2-ns input step to represent the input waveform. The results in terms of maximum slew rate, overshoot, and settling time can be seen in Table I.

The simulated rising edge slew rate is 8% higher than the measure slew rate. The overshoot and settling time show corresponding errors due to a faster simulated response waveform. A list of further test results is given in Table II.

It should be noted that the test circuitry is capable of measuring higher speed signals but is limited by the response characteristics of the DUT. The relatively large noise voltage is due primarily to the noise characteristics of the DUT and output buffer. The harmonic distortion includes components from the DUT, sampling switch, and output buffer. The charge injection error is a high-frequency signal with a fundamental frequency equal to the sampling pulse frequency. It therefore had a negligible effect on our noise and distortion measurements which were made near the signals of interest which have been mixed down to much lower frequencies.

Our measurements were calibrated by comparing our results to direct measurements of the test node using a low capacitance picoprobe. These measurements were somewhat time consuming and may not be practical in some applications. In those cases, such simple calibration circuitry as calibration switches connected to the test node could be added [10].

IV. CONCLUSIONS AND FUTURE WORK

An analog testing procedure has been developed to overcome loading problems associated with high-speed analog signal testing. The signal testing method may be useful for characterizing IC's in both prototype and manufacturing test systems. The procedure is based upon a sequential undersampling approach whereby the signal of interest is mixed down to lower frequencies and then brought off-chip using a low bandwidth amplifier.

In its simplest form, only two components are required on-chip to carry out the test procedure. The first component is an analog switch-and-hold capacitor to sample an input signal. The second component is a low bandwidth amplifier which brings the sampled values off-chip. An IC was designed and tested to demonstrate the procedure. It uses a two-stage opamp as the DUT. The simulate and measure performances of the DUT were in good agreement.

There are a number of areas which can be explored in future work. These include: 1) alternate sample-and-hold configuration and further characterization of sampling circuits, (2) generation of variable frequency low-distortion on-chip sinusoids using a single external signal source, and (3) use of multiple sampling switches in an analog DFT architecture.

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